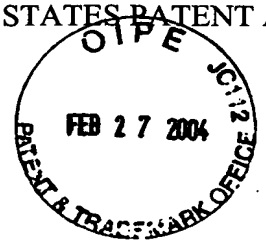
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re the application of:

Xiujun GUAN

Application No. 10/735,104

Filed: December 12, 2003

For: PROCESSOR CORE CLOCK GENERATION CIRCUITS

Group Art Unit: Not Assigned

Examiner: Not Assigned

Atty. Docket No. SUNMP348

Date: February 24, 2004

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450 on February 24, 2004.

Signed: Diane Schwanbeck

Diane Schwanbeck

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicant submits these references in compliance with her duty of disclosure pursuant to 37 CFR §§ 1.56 and 1.97. The Examiner is requested to consider these references and to acknowledge such consideration by initialing the appropriate locations on the attached PTO Form 1449.

This Information Disclosure Statement (IDS) is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This IDS is believed to be filed before the mailing date of a first Office Action on the merits. Accordingly, it is believed that no fees are due in connection with the filing of this IDS. However, if it is determined that any fees are due, then the Commissioner is hereby authorized to charge such fees to Deposit Account 50-0805 (Order No. SUNMP348).

Respectfully submitted,
MARTINE & PENILLA, LLP

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Form 1449 (Modified)	Atty Docket No:	U.S.
	SUNMP348	10/735,104
Information Disclosure	Applicant:	
Statement By Applicant	Xiujun Guan	
	Filing Date:	Group:
(Use Several Sheets if Necessary)	December 12, 2003	

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class
	A					
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					

Foreign Patent Documents

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	L							
	M							
	N							
	O							
	P							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	Q	Hsiang-Hui Chang, Jyh-Woei Lin, Ching-Yuan Yang, Shen-Iuan Liu, "A Wide Range Delay-Locked Loop With a Fixed Latency of One Clock Cycle," IEEE Journal of Solid-State Circuits, Vol. 37, No. 8, August 2002, pp. 1021-1027
	R	Chulwoo Kim, In-Chul Hwang, Sung-Mo (Steve) Kang, "A Low-Power Small-Area ±7.28-ps-Jitter 1-GHz DLL-Based Clock Generator," IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, pp. 1414-1420
	S	

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.